p resistor at the output of the nparator is necessary because f the comparator's open-drain output. The capacitor at the comparator's output smoothes any fast switching the comparator may encounter.

The current consumption of the circuit in **Figure 2** is approximately 1 µA (the current consumption of the comparator) plus the current through R_2 and R_3. The circuit costs less than many dedicated supply-voltage supervisors. **Figure 3** illustrates the performance of the circuit. **Figure 3** is a scope capture of the same battery insertion of **Figure 1**. The top trace is the supply voltage; the next trace is the positive input to the comparator. The negative input to the comparator is the next trace, and the bottom trace is the comparator's output (connected to the microcontroller's reset pin). You can clearly see that the circuit holds the processor in reset until the supply stabilizes. Thus, the perfomance depends not on any predefined supply-voltage level, but rather on stabilization time.

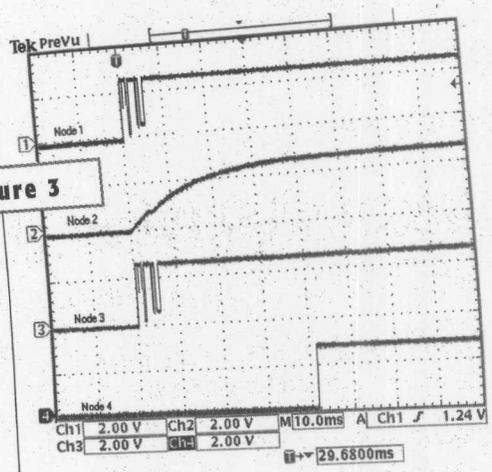

Figure 3

The circuit in Figure 2 enables the processor well after the stabilization of the power-supply voltage.

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Small circuit forms programmable 4- to 20-mA transmitter

Alan Li and Jeritt Kent, Analog Devices, Bellevue, WA

ONE OF THE KEY challenges in the design of 4- to 20-mA current transmitters is the voltage-to-current conversion stage. Conventional transmitters use multiple op amps and transistors to perform the conversion function. These approaches have been around for a long time, but they are usually inflexible, have poor power efficiency, and have limited current compliance. An improved Howland current pump, on the other hand, can be cost-effective, because it addresses the cited problems. In addition, it closely models an ideal current source with the potential for nearly infinite output impedance. **Figure 1** shows the improved Howland-current-pump topology, implemented with a high-resolution DAC, a precision reference, and a high-current op amp. Analyzing the circuit in **Figure 1** (neglecting the loading effects at the output of IC_3), the voltage at V_X is $V_X=(V_{REF}\times D)/2^N$, where D is the decimal equivalent of the DAC's digital code and N is the number of bits.

Analyzing nodes V_L and V_N, you obtain

$$I_L=\frac{V_{OUT}-V_L}{R_3'}-\frac{V_L}{R_1'+R_2'}. \quad (1)$$

$$\frac{V_N-V_X}{R_1}=\frac{V_{OUT}-V_N}{R_2+R_3}. \quad (2)$$

Because V_N and V_P are virtually shorted, you obtain

$$V_N=\frac{R_1'}{R_1'+R_2'}V_L. \quad (3)$$

Substituting V_N and V_{OUT}, I_L becomes

$$I_L=\frac{(R_2+R_3)/R_1}{R_3'}V_X+\frac{(R_1'R_2-R_1R_2')+(R_1'R_3-R_1R_3')}{R_1R_3'(R_1'+R_2')}V_L. \quad (4)$$

Making $R_1=R_1'$, $R_2=R_2'$, and $R_3=R_3'$ simplifies **Equation 4** to

$$I_L=\frac{(R_2+R_3)/R_1}{R_3'}\bullet\frac{V_{REF}\bullet D}{2^N}. \quad (5)$$

According to **Equation 5**, you can use R_3' to set the circuit's sensitivity. You can make R_3' as small as necessary to achieve the desired current and improve the load range. As an alternative, you can make the other resistors large to keep the quiescent current low for high power efficiency. The improved Howland current pump is flexible. It offers both current-sink and -source capability. The input voltage at V_X is polarity-insensitive; you can apply it to either R_1 or R_1'. You can connect the load to the supply rail as a high-side load, or you can refer it to a low-side supply or ground (**Figure 1**). Further, one of the primary advantages of this topology is that the current pump provides poten-

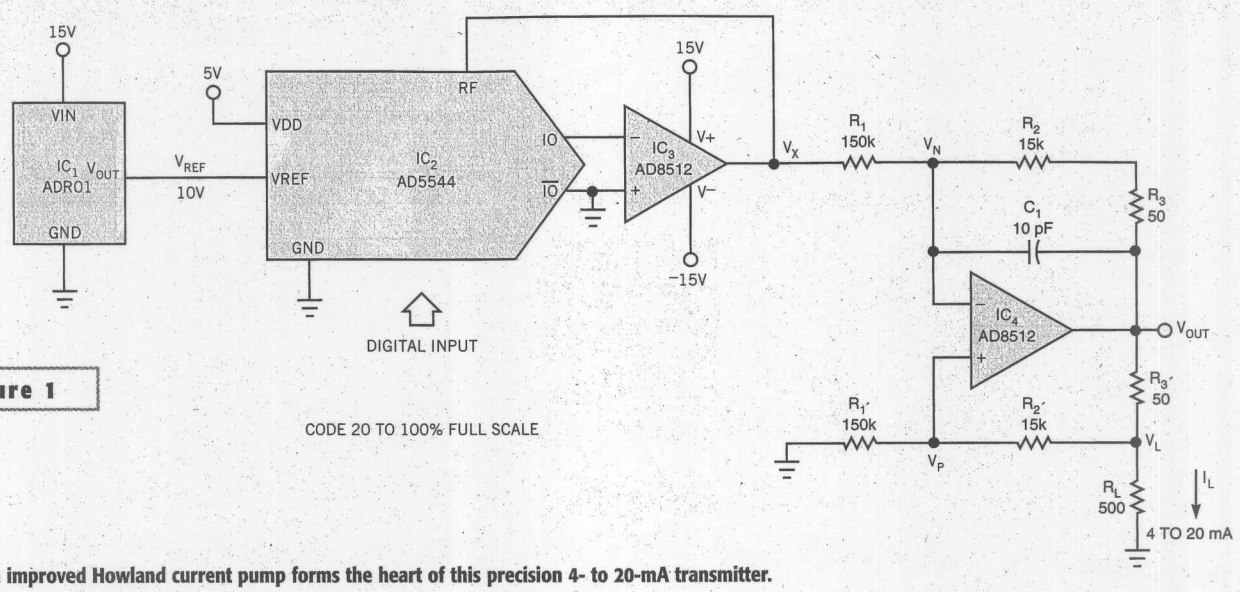

Figure 1

An improved Howland current pump forms the heart of this precision 4- to 20-mA transmitter.

tially *infinite* output impedance, like that of an ideal current source. However, you must pay strict attention to resistor matching. You can see the importance of matching by examining the circuit's output impedance. If you ground all inputs and apply a test voltage at V_L, you can see that

$$Z_{OUT} = \frac{V(t)}{I(t)} = \frac{R_1R_3'(R_1' + R_2')}{R_1'(R_2 + R_3) - R_1(R_2' + R_3')}. \quad (6)$$

Equation 6 shows that, if the resistors are perfectly matched, Z_{OUT} is infinite. Infinite output impedance is a desirable characteristic of a current source because the resistance of the load does not affect the current flowing in the load. On the other hand, if the resistors are not matched, Z_{OUT} can be either positive or negative. Negative Z_{OUT} causes instability because of the existence of a right-half-plane pole in the s-plane domain. Any amount of parasitic capacitance—from poor pc-board layout, op-amp differential capacitance, or both—at the inverting node of IC_4 could cause instability or worse. These parasitics, along with R_1, introduce a zero into the noise-gain transfer function, resulting in a slope of 20 dB per decade. If the noise-gain transfer function of the amplifier intersects with the open-loop response at a slope (rate of closure) equal to or greater than 40 dB per decade and the open-loop gain at the intersection exceeds unity, then the circuit is likely to be unstable. The circuit may ring, show gain peaking, or conditionally oscillate after a step function in the DAC adjustment.

An effective approach to the stability problem is to insert a pole into the noise-gain transfer function by adding a compensation capacitor, C_1. This capacitor creates a pole to keep the rate of closure at 20 dB per decade. Optimum compensation occurs when $R_1C_{PARASITIC} = R_2C_1$. Because $C_{PARASITIC}$ is unknown, you should determine C_1 empirically to obtain optimum results. In general, C_1 in the range of some tenths of a picofarad to a few picofarads satisfies compensation requirements. Note that optimum compensation attempts to balance the fact that a small C_1 cannot compensate for all possible causes of oscillation, whereas large values of C_1 could adversely affect the settling time of any DAC. Consider the following design objectives: 16-bit programmability, four channels, small form factor, a maximum ground-referred load of 500Ω with 10V compliance, 90% minimum efficiency, and 50-mW maximum dissipation from each resistor.

Given the requirements of small form factor and high precision, the design in **Figure 1** uses IC_2, the a 16-bit current-output AD5544 DAC, with an external op amp instead of a voltage-output DAC. You face some important trade-offs in deciding whether to use a current-output or a voltage-output DAC. Current-output devices typically cost less than voltage-output DACs. The design must convert the current to a voltage to run the current pump, and the external op amp determines the accuracy of this conversion. Thus, you have control of the amount of accuracy as your application requires. Voltage-output DACs generally cost more than current-output devices because the current-to-voltage conversion takes place in the package, entailing the inclusion of an op amp. Al-

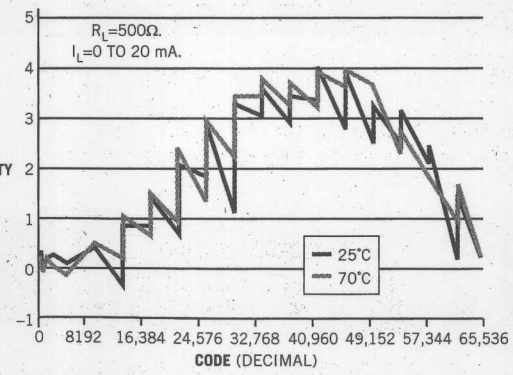

Figure 2

Integral-nonlinearity errors from the circuit in Figure 1 don't exceed 4 LSBs at 16-bit resolution.

though a voltage-output DAC reduces component count in this design, you have to accept a particular accuracy figure based on the specifications of the op-amp buffer inside the DAC. Both approaches typically require an external reference. In the end, a current-output approach yields the highest accuracy at comparable cost and board space.

Although IC_3, which performs the current-to-voltage conversion, can be almost any precision op amp using ±15V supplies, IC_4 requires adequate current-driving capability to handle the maximum 20-mA load. The improved Howland current pump is insensitive to load-resistance perturbations. Only IC_4's supply voltages limit the compliance voltage. A 500Ω load, for example, can place V_L as high as 10V at 20-mA load current. This scenario sets V_{OUT} at 11V, requiring the op amp to swing within 4V of the positive rail. The AD8512 dual op amp can drive 20 mA into a 500Ω load using ±15V supplies. However, IC_4's output-voltage swing is likely to limit resistive loads to 500Ω in this application. This design uses the 10V ADR01 reference because it is precise and compact.

To minimize the power in the resistors, you start with $R_3'=50\Omega$. R_3' is in the direct load-current path, and it carries just slightly more current than the load, assuming $R_2'+R_1'>>R_L$. At the 20-mA peak current, the power dissipation is just above 20 mW. With the limited headroom between the supply and the compliance voltages, you should scale the ratio between R_2 and R_3 such that the additional gain does not saturate IC_4. As a result, you should choose R_2 to be 10 times smaller than R_1. Using **Equation 5** and the resistance-matching criteria, you obtain the following values: $R_1=R_1'=150$ kΩ; $R_2=R_2'=15$ kΩ, and $R_3=R_3'=50\Omega$. It's desirable to add a 1- to 10-pF capacitor, C_1, to the negative-feedback path to avoid possible oscillation arising from eventual resistor mismatch.

A 16-bit, programmable, 4- to 20-mA current transmitter theoretically has 0.3-µA resolution. The actual measured performance of the circuit in **Figure 1** shows that the worst-case integral-nonlinearity error is approximately 4 LSBs. This error is equivalent to 1.2 µA, or 0.006% total system error, well within most systems' requirements. **Figure 2** shows the measured results at 25 and 70°C.

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High-side current sensor monitors negative rail

Ken Yang, Maxim Integrated Products, Sunnyvale, CA

All dedicated current-sense amplifiers provide high-side sensing on a positive supply, but you can adapt such circuits for monitoring a negative supply (**Figure 1**). The positive-supply pin, V+, connects to the system's positive supply, and the ground pin, GND, connects to the negative supply, V_{EE}. That arrangement monitors the negative supply and provides a positive output voltage for the external interface—typically, an A/D converter. The RS+ pin of the current-sense amplifier, IC_1, connects to the load, and the RS− pin connects to the negative supply. IC_1's current-source output drives a current that is proportional to load current flowing to ground, not to the GND pin. Output resistor R_{OUT} converts the current to a voltage, which an optional ADC then digitizes.

Saturation in the internal transistors, which occurs at approximately ((V+)−1.2V), limits the maximum output voltage. Thus, V+ must exceed the full-scale output by at least 1.2V. If, for instance, the full-scale output is 1V, then V+≥2.2V. To meet the device's maximum and minimum operating voltages, $0\geq V_{EE}\geq-(32-V+)$, and $((V+)-V_{EE}))\geq 3V$. **Figure 2** shows the variation of current measurement accuracy with load current.

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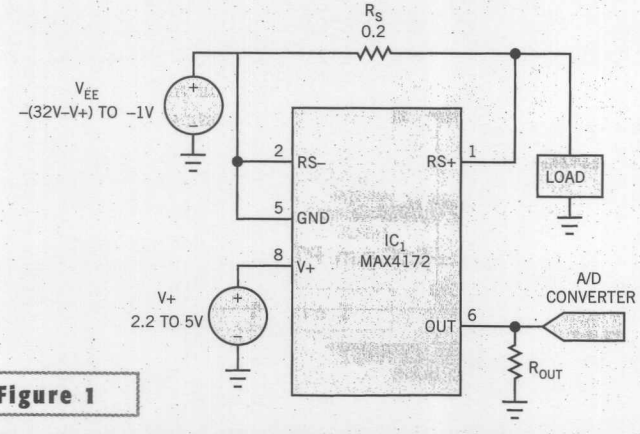

Figure 1

Connecting this positive-supply monitor allows it to monitor a negative current and generate a positive output voltage for the ADC.

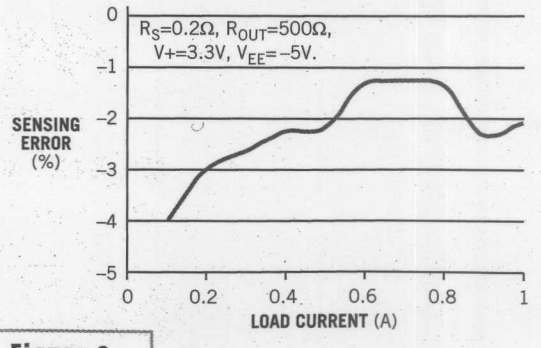

Figure 2

The current-sensing error of the circuit in Figure 1 varies with load current.